WE CLAIM:

1. A method for depositing an epitaxial Ge-containing layer, comprising

heating a single crystal Si structure to a first temperature;

cooling the single crystal Si structure to a second temperature during a cooling time period;

contacting the single crystal Si structure with a surface active compound during at least a portion of the cooling time period; and

depositing an epitaxial layer over the single crystal Si structure at the second temperature.

2. The method of Claim 1, wherein the first temperature is about 450°C or higher.

3. The method of Claim 1, wherein heating the single crystal Si structure comprises removing a native oxide.

4. The method of Claim 1, wherein heating the single crystal Si structure comprises driving off surface contaminants.

5. The method of Claim 4, wherein driving off surface contaminants comprises hydrogen baking at about 600°C or greater.

6. The method of Claim 1, wherein depositing the epitaxial layer comprises heteroepitaxial deposition.

7. The method of Claim 6, wherein the epitaxial layer has a Ge content in the range of about 50 atomic % to about 100 atomic %.

8. The method of Claim 6, wherein the epitaxial layer has a Ge content of about 99 atomic % Ge or higher.

9. The method of Claim 8, further comprising depositing a relaxed SiGe alloy layer over the epitaxial layer.

10. The method of Claim 9, wherein the SiGe alloy layer is graded from a high Ge content at an interface with the epitaxial layer to a lower Ge content at an upper surface.

11. The method of Claim 6, wherein depositing the epitaxial layer comprises contacting the single crystal Si structure with a germanium source selected from the group consisting of germane, digermane and trigermane.

12. The method of Claim 1, wherein the epitaxial layer is a Si_xGe_{1-x} layer, where x is in the range of zero to one.

13. The method of Claim 1, wherein the first temperature is about 600°C or higher.

14. The method of Claim 13, wherein the second temperature is in the range of about 300°C to about 450°C.

15. The method of Claim 1, wherein the surface active compound is selected from the group consisting of silane, disilane, trisilane, chlorosilane, dichlorosilane, trichlorosilane, and tetrachlorosilane.

16. The method of Claim 15, wherein the surface active compound is selected from the group consisting of chlorogermane, dichlorogermane, trichlorogermane, tetrachlorogermane,

17. The method of Claim 1, wherein the surface active compound is dichlorosilane.

18. The method of Claim 1, wherein heating the single crystal Si structure comprises epitaxial Si deposition.

19. The method of Claim 1, wherein cooling the single crystal Si structure is conducted in a single wafer reactor.

20. The method of Claim 1, wherein cooling the single crystal Si is conducted in a batch furnace.

21. The method of Claim 1, wherein contacting comprises providing the surface active compound at a rate of about 1 sccm to 500 sccm.

22. The method of Claim 1, wherein contacting comprises providing the surface active compound at a rate of about 1 sccm to 50 sccm.

23. The method of Claim 1, wherein cooling the single crystal Si structure is conducted under a pressure between about 200 mTorr and 760 Torr.

24. The method of Claim 1, wherein cooling the single crystal Si structure is conducted under a pressure between about 1 Torr and 100 Torr.

25. The method of Claim 1, wherein cooling comprises cooling from the first temperature to an intermediate temperature and contacting comprises introducing the surface

active compound to the single crystal Si structure at the intermediate temperature and continuing to cool from the intermediate temperature to the second temperature.

26. The method of Claim 25, wherein the intermediate temperature is between about 600°C and 800°C.

27. The method of Claim 25, wherein the intermediate temperature is greater than about 650°C.

28. The method of Claim 1, wherein the surface active compound is selected from the group consisting of Si precursors and Ge precursors.

29. The method of Claim 28, wherein the surface active compound is selected from the group consisting of a silane, a germane, an organosilane, a halogermane and a halosilane.

30. The method of Claim 28, wherein contacting comprises depositing less than about 500 Å during cooling prior to depositing the epitaxial layer.

31. A process for forming a strained semiconductor layer over a substrate, comprising:

forming a relaxed epitaxial Ge layer over the substrate;

depositing a relaxed epitaxial SiGe alloy layer onto the relaxed epitaxial Ge layer, the relaxed SiGe alloy layer having an increasing Si content with distance from an interface with the relaxed epitaxial Ge layer; and

depositing a strained epitaxial semiconductor layer onto the relaxed epitaxial SiGe alloy layer.

32. The process of Claim 31, wherein forming the relaxed epitaxial Ge layer comprises cooling the substrate from a high temperature to a Ge deposition temperature while supplying a Si or Ge precursor to the substrate.

33. The process of Claim 32, wherein depositing the strained epitaxial semiconductor layer comprises depositing a strained Ge layer.

34. The process of Claim 33, wherein depositing the strained epitaxial semiconductor layer further comprises depositing a strained epitaxial Si layer onto the strained epitaxial Ge layer.

35. The process of Claim 33, wherein depositing the strained epitaxial Ge layer comprises cooling the substrate from a SiGe alloy deposition temperature to a Ge deposition temperature while supplying a Si or Ge precursor to the substrate.

36. The process of Claim 33, further comprising depositing a Si cap layer over the strained epitaxial Ge layer using trisilane as a silicon precursor.

37. A semiconductor structure, comprising

a single crystal Si structure;

an epitaxial Ge layer deposited on the single crystal Si structure; and

a SiGe alloy layer deposited on the epitaxial Ge layer.

38. The semiconductor structure of Claim 37, wherein the SiGe alloy layer is at least partially relaxed.

39. The semiconductor structure of Claim 38, further comprising a strained epitaxial Si layer overlying the $Si_{1-x}Ge_x$ layer.

40. The semiconductor structure of Claim 37, wherein the epitaxial Ge layer has a thickness in the range of from about 10 Å to about 1 micron.

41. The semiconductor structure of Claim 40, wherein the epitaxial Ge layer has a thickness in the range of from about 10 Å to about 500 Å.

42. The semiconductor structure of Claim 37, wherein the SiGe alloy layer has a lower dislocation density than a comparable $Si_{1-x}Ge_x$ layer deposited directly onto the epitaxial Si layer.

43. The semiconductor structure of Claim 37, wherein the SiGe alloy layer has a dislocation determined by the etch pit decoration method of less than about 10^7 defects/cm^2.

44. The semiconductor structure of Claim 37, wherein the SiGe alloy layer has a dislocation determined by the etch pit decoration method of less than about 10^5 defects/cm^2.

45. The semiconductor structure of Claim 37, wherein the SiGe alloy layer is graded.

46. The semiconductor structure of Claim 45, wherein the SiGe alloy layer is graded from a high Ge content at an interface with the epitaxial Ge layer to a lower Ge content at an upper surface.

47. The semiconductor structure of Claim 46, further comprising a strained semiconductor layer directly overlying the SiGe alloy layer.

48. The semiconductor structure of Claim 46, further comprising a strained Ge epitaxial layer directly overlying the SiGe alloy layer and a strained Si epitaxial layer directly overlying the strained Ge epitaxial layer.

49. An epitaxial semiconductor deposition system, comprising

a deposition chamber configured to support at least one workpiece;

a surface active compound source vessel comprising a surface active compound, the surface active compound source vessel being operatively connected to the chamber to allow the surface active compound to flow into the chamber;

a germanium source vessel comprising a germanium precursor, the germanium source vessel being operatively connected to the chamber to allow the germanium precursor to flow into the chamber;

a heater configured to heat the at least one workpiece within the chamber; and

controls operatively connected and set to control flow of the surface active compound and the germanium precursor, and to control the temperature of the workpiece to conduct in sequence a high temperature process step, a cooling step and a low temperature Ge-containing epitaxial deposition step, wherein the controls provide the surface active compound to the at least one workpiece during at least a lower portion of the cooling step.

50. The epitaxial semiconductor deposition system of Claim 49, further comprising a silicon source vessel, wherein the silicon precursor comprises a compound selected from the group consisting of silane, disilane and trisilane.

51. The epitaxial semiconductor deposition system of Claim 50, wherein the controls are further connected and set to control flow of the silicon precursor into the chamber to deposit a Si-containing layer during the first high temperature step.

52. The epitaxial semiconductor deposition system of Claim 50, wherein the controls are further connected and set to control flow of the silicon precursor into the chamber to deposit an epitaxial SiGe alloy layer over the workpiece after cooling.

53. The epitaxial semiconductor deposition system of Claim 52, wherein the controls are set to deposit an epitaxial Ge layer over the workpiece after cooling and to deposit the epitaxial SiGe alloy over the epitaxial Ge layer.

54. The epitaxial semiconductor deposition system of Claim 49, wherein the surface active compound is selected from the group consisting of chlorogermane, dichlorogermane, trichlorogermane, tetrachlorogermane, chlorosilane, dichlorosilane, trichlorosilane, tetrachlorosilane, methylsilane, dimethylsilane, trimethylsilane and tetramethylsilane.

55. The epitaxial semiconductor deposition system of Claim 49, wherein the surface active compound is selected from the group consisting of Si precursors and Ge precursors.

56. The epitaxial semiconductor deposition system of Claim 55, wherein the surface active compound is dichlorosilane.

57. The epitaxial semiconductor deposition system of Claim 49, wherein the germanium precursor is selected from the group consisting of germane, digermane and trigermane.

58. The epitaxial semiconductor deposition system of Claim 49, wherein the chamber is configured for simultaneously accommodating a batch of workpieces.

59. The epitaxial semiconductor deposition system of Claim 58, wherein the chamber is configured to simultaneously accommodate 50-100 wafers.

60. The epitaxial semiconductor deposition system of Claim 58, wherein the controls are set to maintain a deposition pressure between about 0.001 Torr and 760 Torr.

61. The epitaxial semiconductor deposition system of Claim 49, wherein the controls are set to provide between about 1 sccm and 500 sccm of the surface active compound during at least the lower portion of the cooling step.

62. The epitaxial semiconductor deposition system of Claim 49, wherein the chamber is configured process a single wafer at a time.

63. The epitaxial semiconductor deposition system of Claim 62, wherein the controls are set to maintain a deposition pressure between about 1 Torr and 100 Torr.

64. A method for depositing an epitaxial Ge layer, comprising

providing a substrate having a single crystal semiconductor surface disposed within a reactor;

heating the substrate to a first temperature of about 450°C or higher;

cooling the substrate to a second temperature during a cooling time period, the reactor having a reactor pressure in the range of about 0.001 Torr to about 760 Torr during said cooling period;

contacting the single crystal semiconductor surface with a surface active compound selected from the group consisting of Si precursors and Ge precursors during at least a portion of the cooling time period; and

depositing an epitaxial Ge layer onto the single crystal semiconductor surface at the second temperature.

65. The method of Claim 64, wherein depositing the epitaxial Ge layer comprises contacting the single crystal Si substrate with a germanium source selected from the group consisting of germane, digermane and trigermane.

66. The method of Claim 64, wherein the surface active compound is selected from the group consisting of silane, disilane, trisilane, chlorosilane, dichlorosilane, trichlorosilane, and tetrachlorosilane.

67. The method of Claim 66, wherein the surface active compound is dichlorosilane.

68. The method of Claim 64, wherein the reactor pressure is in the range of about 1 Torr to about 100 Torr during said cooling period.

69. The method of Claim 64, wherein the epitaxial Ge layer has a surface roughness of about 25 Å rms or less, as measured by atomic force microscopy.

70. The method of Claim 64, wherein the epitaxial Ge layer has a threading dislocation density of about 10^7 defects/cm^2 or less as measured by an etch pit decoration method.

71. The method of Claim 64, wherein the epitaxial Ge layer is deposited at a rate of at least about 300 Å per minute.

72. The method of Claim 64, wherein the epitaxial Ge layer is deposited at a rate of at least about 500 Å per minute.

73. The method of Claim 64, further comprising heating the epitaxial Ge layer to a third temperature and depositing additional epitaxial Ge onto the epitaxial Ge layer.

74. A method for depositing an epitaxial Ge layer, comprising

providing a single crystal Si substrate disposed within a single wafer reactor;

heating the single crystal Si substrate to a first temperature of about 600°C or higher;

cooling the single crystal Si substrate to a second temperature of about 450°C or less during a cooling time period, the reactor having a reactor pressure in the range of about 1 Torr to about 100 Torr during said cooling time period; and

depositing an epitaxial Ge layer over the single crystal Si substrate at the second temperature.

75. The method of Claim 74, further comprising contacting the single crystal Si substrate with a compound during at least a portion of the cooling time period, the compound being selected from the group consisting of silicon and germanium precursors.

76. The method of Claim 74, further comprising depositing a relaxed SiGe buffer layer over the epitaxial Ge layer and depositing a strained semiconductor layer thereover.

77. The method of Claim 76, wherein the strained semiconductor layer comprises a strained Ge layer and a strained Si layer to form a dual channel in a transistor device.

78. A multi-layer semiconductor structure comprising:

an underlying single crystal silicon structure; and

an overlying epitaxial germanium layer directly on the silicon structure, having an as-deposited threading dislocation density of about 10^7 defects/cm^2 or less, as measured by an etch pit decoration method, and an as-deposited surface roughness of about 20 Å rms or less, as measured by atomic force microscopy across at least a 10 micron x 10 micron window.

79. The multilayer semiconductor structure of Claim 78, wherein the overlying epitaxial germanium layer has a threading dislocation density of about 10^5 defects/cm^2 or less as measured by an etch pit decoration method.

80. The multilayer semiconductor structure of Claim 78, wherein the overlying epitaxial germanium layer has a thickness in the range of about 10 Å to about 1 micron.

81. The multilayer semiconductor structure of Claim 78, wherein the underlying single crystal silicon structure is a wafer.

82. The multilayer semiconductor structure of Claim 78, wherein the epitaxial germanium layer has a surface roughness of about 10 Å rms or less.

83. The multilayer semiconductor structure of Claim 78, wherein the epitaxial germanium layer has a thickness between about 10 Å and 500 Å.